The Correction Method for Power Noise in Digital Class D Power Amplifiers

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***Abstract*—In a digital class D power amplifier, the distortion is introduced into the input signal being amplified in power stage, due to the effect of power supply noise. A method used to eliminate the distortion is presented in the paper. This method is adding correction factors to all integrators of Delta-Sigma modulator, and introducing power supply noise to the input of the class D power amplifier and Delta-Sigma modulator. A design example with the method is presented, and the simulation results indicate this method can eliminate the error introduced by power stage.**

***Index Terms*—power stage, power supply noise, Delta-Sigma modulator, digital class D power amplifier, PWM**

I. INTRODUCTION

Class D power amplifiers become more and more attractive in the field of consumer electronics nowadays, because their power supply efficiency is significantly higher than traditional linear counterparts such as class A, B and AB power amplifiers. High efficiency of class D power amplifiers is due to their power MOSFETs in power stage acting as switches with very small power dissipation. At present, most class D power amplifiers process their input signals with analog circuit, so it's difficult to design them and these amplifiers are sensitive to various kinds of noise [1][2]. In order to overcome the drawbacks of analog class D power amplifiers, digital class D power amplifiers are becoming a hot spot of present research.

In this paper, a system architecture of digital class D power amplifier is presented firstly, the system include a digital PWM (pulse width modulator) block, a single-ended power stage and a analog low pass filter. Because of the nonlinearity of digital PWM block and the effect of power supply noise in power stage, error will be introduced in the power amplifier [3]. In [4], we have corrected the nonlinearity of the digital PWM block, and the nonlinearity can be eliminated after correction. Based on the early works, a method of error correction for power stage is proposed in this paper to eliminate the error introduced by power supply noise. Then a digital class D power amplifier with the method is designed and simulated. At last, conclusions are given.

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II. THE SYSTEM ARCHITECTURE OF DIGITAL CLASS D POWER AMPLIFIER

The proposed digital class D power amplifier architecture is shown in "Fig. 1". It's made up of a digital PWM block, a single-ended power stage and a LC low pass filter. The digital PWM block consists of a Delta-Sigma modulator and a PWM (pulse width modulation) generator. Compared with analog class D power amplifier, the digital class D power amplifier has an all-digital PWM block, so it has the characteristics of high anti-interference and good portability [5][6]. Compared with the power amplifier with H-bridge power stage, the power amplifier with single-ended power stage can cut down half of driver circuit and power MOSFETs. To implement the power amplifier easily, the Delta-Sigma modulator with noise-shaping technology is added in the system to reduce the working frequency of digital PWM block greatly while SNR of output signal is remained [7]. (assuming 4th-order Delta-Sigma modulator in "Fig. 1")

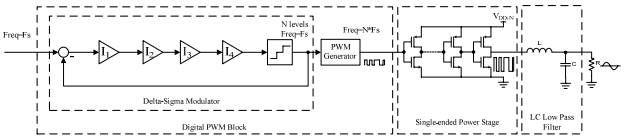

Fig. 1. The proposed digital class D power amplifier architecture.

Although the digital PWM block shown in Fig. 1 is easy to implement, nonlinear error will be introduced in the block due to the nonlinearity of the block. In [4], a method of error correction is presented. The method makes digital PWM block linearized, through adding different correction factors to all integrators in Delta-Sigma modulator according to the output of Delta-Sigma modulator. In the system, error is not only introduced by the nonlinearity of the digital PWM generator, but also introduced by the power supply noise in power stage. Due to the effect of power supply noise in power stage, the

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distortion is introduced into the input signal being amplified in power stage [8]. So a method is needed to correct the error introduced by power supply noise in power stage.

III. The Method Of Error Correction For Power Stage

The power supply with noise V_{DD+N} shown in "Fig. 1" can be normalized as [9]:

$$V_{normalized+N} = \frac{V_{DD+N}}{V_{DD}} = 1 + V_N = 1 + N\ \boldsymbol{sin}(2\pi f_N t) \quad (1)$$

In the above equation, V_{DD} is the amplitude of the ideal noise-free power supply, V_N is the normalized power supply noise, f_N is the frequency of the power supply noise, and N is the normalized amplitude of the power supply noise.

To correct the error introduced by power supply noise, the power stage can be divided into two blocks: distortion block and amplification block. The input of the power stage is distorted in distortion block before amplified. Hence Fig. 2 is obtained, and "Fig. 2" equals "Fig. 1".

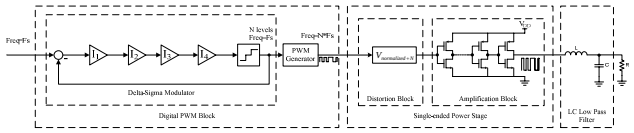

Fig. 2. The system architecture with the decomposed power stage.

In "Fig. 2", the digital PWM block is assumed to be linear firstly. Because of the structure of single-ended power stage, the normalized power supply noise V_N is needed to be subtracted from the input of the system real-timely to offset the energy of the power supply noise, i.e. the input signal of the system after correction is the difference between the original input signal of the system and the normalized power supply noise. Besides that, a method of the pre-correction is used to correct the IMD (inter-modulation distortion) introduced by the power supply noise against the input the system. This method is comparing the input with the output of the distortion block, obtaining the difference, and then putting it through an integrator (the integrator works opposite to the digital PWM generator), as a feedback into the input of the system. So the input of the system can pre-correct the error produced in the power stage. The system with the above methods is shown in "Fig. 3".

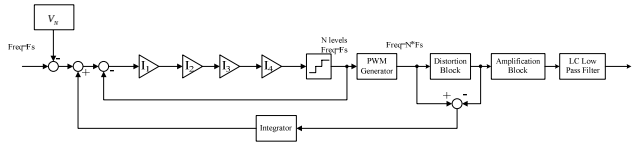

Fig. 3. The system structure with the method of power stage error correction.

Then "Fig. 3" can be equivalently transformed into "Fig. 4":

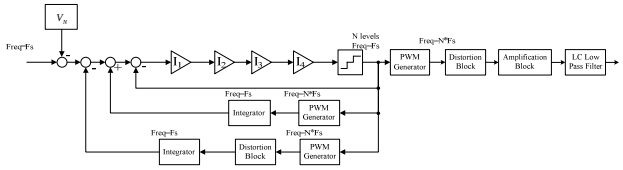

Fig. 4. The system structure equaling the structure of Fig. 3.

Because the integrator works opposite to the digital PWM generator, a signal goes through the two blocks, and then the output becomes the primary signal. Because the frequency Fs is greatly greater than the frequency of power supply noise f_N commonly, the output of the distortion block can be considered the same at the time interval $\frac{1}{Fs}$. So a signal gone through PWM generator, distortion block and integrator can equal the signal gone through distortion block only. Hence "Fig. 5" can equal "Fig. 4".

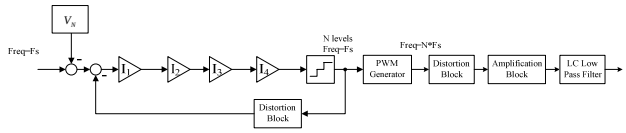

Fig. 5. The system structure equaling the structure of Fig. 4.

In [4], the state equation of digital PWM block shown in Fig. 1 is analyzed to get the method of the nonlinearity of the digital PWM block. Compared with the structure of digital PWM block in "Fig. 1", the structure of digital PWM block changes now, so a new method of the nonlinearity of the digital PWM block is needed to analyze.

In" Fig.5" the Delta-Sigma modulator can be described as:

$$I_{n+1} = AI_n + B_y Y_n D_n + B_x X_n \quad (2)$$

$$Y_{n+1} = Q(I_{n+1}) \quad (3)$$

$$X = 0,\ I_{n+1} = AI_n + B_y Y_n D_n \quad (4)$$

$$Y_{n+1} = Q(I_{n+1}) \quad (5)$$

Because the order of the Delta-Sigma modulator in "Fig. 5" is 4, in above functions, 'I' is the vector representation of the integrator, 'Y' is the output of the quantizer, 'X' is the input of the Delta-Sigma modulator, i.e. the difference between the input of the system and the normalized power supply noise, 'YD' is the output of the distortion block in Delta-Sigma modulator and 'Q' is the quantizer function. It is important to notice that 'I', 'B_x' and 'B_y'are all vectors (of size 4 by 1), and 'Y' and 'D' are scalars and A is a matrix of size 4 by 4.

One method of avoiding the nonlinear distortion produced

in PWM generator is to include the PWM generator inside the loop of the Delta-Sigma modulator. After that, the new loop should not have any nonlinear distortion because of its high open-loop gain in the signal band. But PWM generator can't be moved into the Delta-Sigma modulator's loop directly, because the output of the PWM generator is of a much higher clock resolution than the input of the Delta-Sigma modulator.

So an upsampling block and a downsampling block are added to the system, and the new system is shown in "Fig. 6".

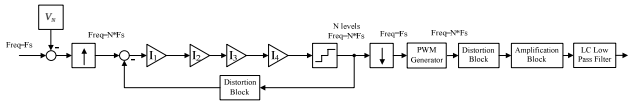

Fig. 6. The system structure inlcuding upsampling block and downsampling block.

The following equations describe the above Delta-Sigma modulator that runs N times faster (taking N=4, to simplify):

$$I_n^2 = aI_n^1 + b_y Y_n^1 D_n^1 \tag{6}$$

$$I_n^3 = aI_n^2 + b_y Y_n^2 D_n^2 \tag{7}$$

$$I_n^4 = aI_n^3 + b_y Y_n^3 D_n^3 \tag{8}$$

$$I_{n+1}^1 = aI_n^4 + b_y Y_n^4 D_n^4 \tag{9}$$

So

$$I_{n+1}^1 = a^4 I_n^1 + \sum_{p=1}^{4} a^{4-p} b_y Y_n^p D_n^p \tag{10}$$

Now satisfying the following conditions will make the system in "Fig. 6" equal the system in "Fig. 5": $I_n^1 = I_n$, $Y_n^{k_1} = Y_n$ (k_1 can be anyone in 0~4), $Y_n^k = 0$ ($k \neq k_1$), $D_n^p = D_n$. So $a^4 = A$, $a^{4-k_1} b_y Y_n^{k_1} D_n^{k_1} = B_y Y_n D_n$, $b_y = a^{k_1-4} B_y$.

As planned, in "Fig. 6", the output of the PWM generator is of the same clock resolution with the input of the sigma-delta modulator. So the PWM generator can be moved into the Delta-Sigma modulator's loop. The new system is shown in "Fig. 7".

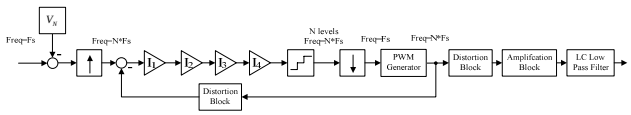

Fig. 7. The system with PWM generator moved into the Delta-Sigma modulator's loop.

The loop's state equation in "Fig. 7" is the same as the Delta-Sigma modulator's state equation in "Fig. 6", but the meaning of Y is different.

In "Fig. 7", the working frequency of Delta-Sigma modulator is too high to implement. So the system in Fig. 8 is given. This system equals the system in Fig. 8, through adding correction factors to all integrators in Delta-Sigma modulator. The correction factors are equal to the difference between the state equation of the loop in Fig. 7 and in Fig. 6:

$$Corr = \sum_{p=1}^{4} a^{k_1-p} B_y Y_n^p D_n^p - B_y Y_n D_n \tag{11}$$

In Eq. (11), Y is the output of the PWM generator.

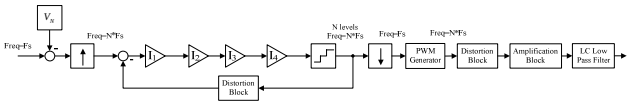

Fig. 8. The system adding the correction factors.

Deleting the upsampling block and downsampling block, the new system equaling the system in "Fig. 8" is shown in "Fig. 9".

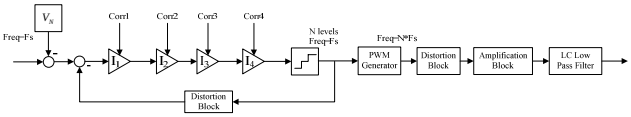

Fig. 9. The system deleting the upsampling block and downsampling block.

The correction factors calculated from Eq. (11) are added to the system in "Fig. 9", which can correct the error introduced by power supply noise in power stage on the premise of ensuring the linearity of the digital PWM Block.

IV. Design Example

In this section, the proposed method of error correction for power stage is verified by a digital audio class D power amplifier system shown in "Fig. 10". The error correction block in "Fig. 10" can correct the error introduced by the nonlinearity of the digital PWM block and power supply noise in power stage.

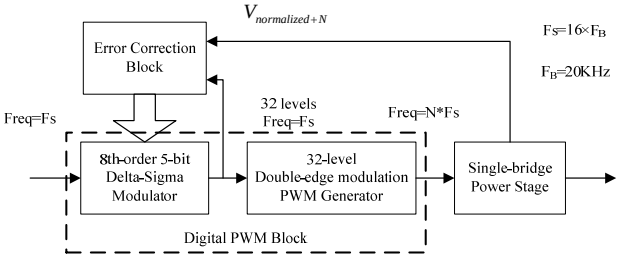

Fig. 10. A digital audio class D power amplifier system.

The master clock frequency of the proposed digital audio class D power amplifier is 12288KHz, the passband of input signal is 48KHz, and digital PWM generator is 32-level, so a 8×interpolation filter and a 5-bit sigma-delta modulator are needed in the system.

A. Interpolation Filter

Interpolation filters can oversample their input signals. The passband ripple of the proposed 8×interpolation filter is required to be less than 0.0001dB and the stopband attenuation of the proposed 8×interpolation filter is

required to be greater than 100dB to preserve the informantion of its input signal in baseband. In order to implement the 8×interpolation filter easily, three half-band 2×interpolation filters are cascaded to construct it.

To reduce the difficulty of design, the three half-band 2×interpolation filters are designed in the structure of tapped cascaded interconnection of identical subfilters to achieve above desired design specifications . The main structures of the three half-band 2×interpolation filters are same and are all shown in "Fig.11".

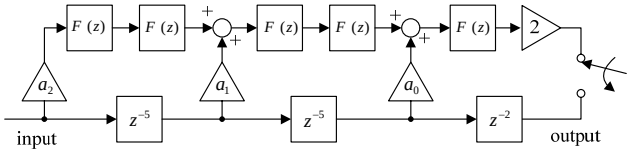

Fig.11. The main structures of the three half-band 2×interpolation filters.

For the first half-band 2×interpolation filter, the structure of its subfilter F(z) in "Fig.11" is shown in "Fig.12". All coefficients in "Fig.12" are encoded in CSD coding.

For the second half-band 2×interpolation filter, the structure of its subfilter F(z) in "Fig.11" is shown in "Fig.13". All coefficients in "Fig.13" are encoded in CSD coding.

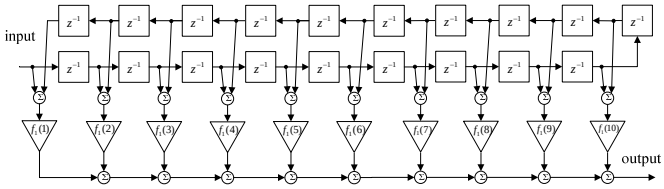

Fig. 12.The structure of the subfilter in thefirst half-band 2×interpolation filter.

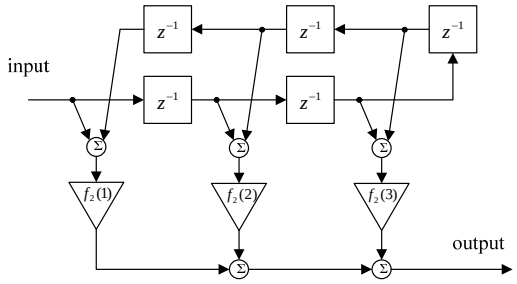

Fig.13. The structure of the subfilter in the second half-band 2×interpolation filter.

For the third half-band 2×interpolation filter, the structure of its subfilter F(z) in "Fig.11" is shown in "Fig.14". All coefficients in "Fig.14" are encoded in CSD coding.

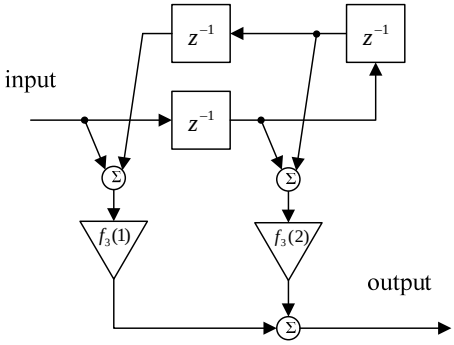

Fig.14. The structure of the subfilter in the third 2×interpolation half-band filter.

The amplitude-frequency response of the entire 8×interpolation filter is shown in "Fig.15". In "Fig.15", the passband ripple of the proposed 8×interpolation filter is less than 0.0001dB, and the stopband attenuation of the proposed 8×interpolation filter is 105dB.

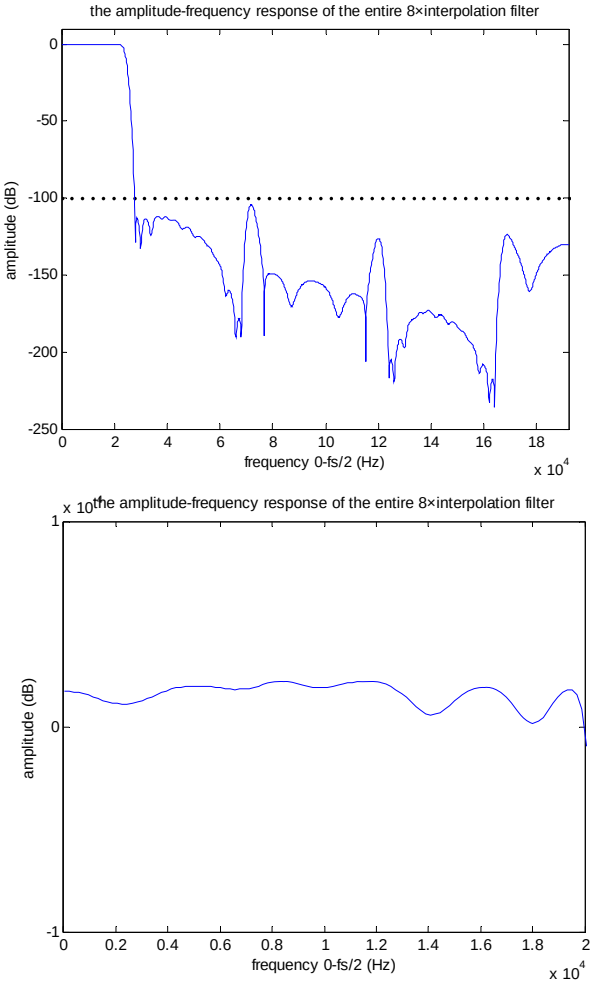

Fig.15.The amplitude-frequency response of the entire 8×interpolation filter.

B. *Sigma-delta Modulator*

An interpolating structure high-order 5-bit sigma-delta modulator is desiged in this paper for achieving a good noise-compression effect. The key of the design of a sigma-delta modulator is designing its noise transfer function (NTF). The interpolating structure sigma-delta modulator can distribute all zore points of its NTF among signal bandwidth uniformly, not at direct current (dc) only, to achieve a good noise-compression effect. But 3rd-order and higher-order sigma-delta modulator is likely to be unstable, especially when its input signals with fairly large amplitude input the sigma-delta modulator. According to [7], the out-of-band gain of the NTF of a sigma-delta modulator is inversely proportional to the stability of the modulator and directly proportional to the degree of noise-compression. So a 8th-order 5-bit sigma-delta modulator is designed in this paper through choosing different order of the modulator continually and optimizing zero point and pole point of its NTF. The NTF of the proposed sigma-delta modulator can be expressed as:

$$NTF(z)=\frac{(z-1)^2\cdot(z^2-1.969z+1)\cdot(z^2-1.922z+1)\cdot(z^2-1.891z+1)}{(z^2-1.61z+0.6879)\cdot(z^2-0.687z+0.2225)\cdot(z^2-1.162z+0.4709)\cdot(z^2-1.634z+0.8673)}$$

The amplitude-frequency response of the NTF is shown in “Fig.16”. The structural model of the sigma-delta modulator derived from the NTF is shown in “Fig.17”

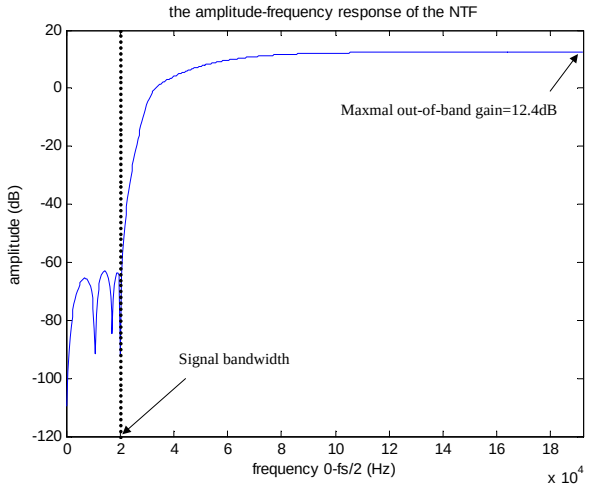

Fig.16. The amplitude-frequency response of the NTF of the sigma-delta modulator.

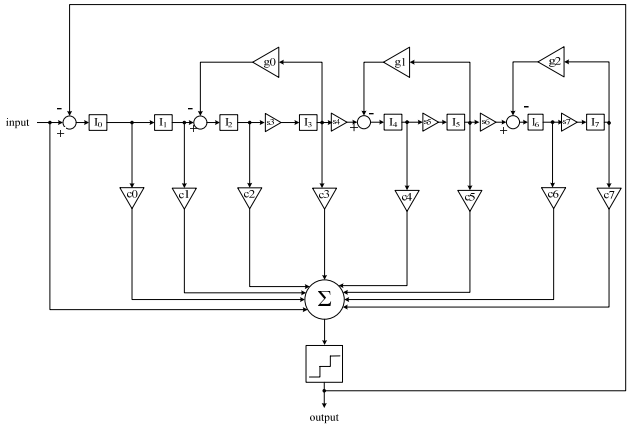

Fig.17. The structural model of the sigma-delta modulator.

The effect of power supply noise in power stage and the nonlinearity of the digital PWM generator can be corrected by adding correction factors to integrators in sigma-delta modulator as described in section Ⅲ.

Compared to the correction effect of the correction factors added in these integrators I1, I2, I3 in the sigma-delta modulator, the correction effect of the correction factors added in these integrators I0 I4, I5, I6, I7 is very small. So the correction factors added in these integrators I0 I4, I5, I6, I7 can be omited, The structure of the sigma-delta modulator with error correction is shown in “Fig.18”.

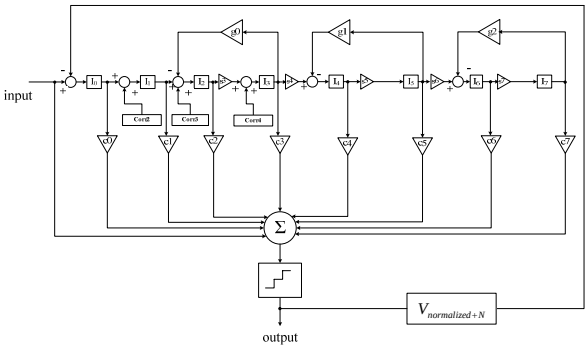

Fig18. The structure of the sigma-delta modulator with error correction

C. PWM Generator

A digital double-edge PWM generator is designed in this paper to obtain a good total harmonic distortion (THD). Thirty-three kinds of pulse wave patterns can be outputed from the digital PWM generator, and every pulse wave pattern corresponds to every output of the sigma-delta modulator designed in above section. The function diagram of the digital double-edge PWM generator is shown in “Fig.19”.

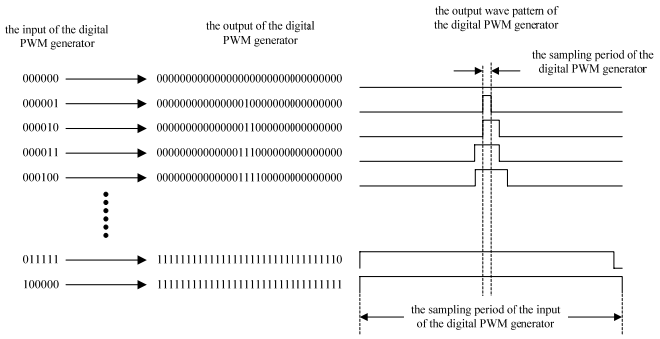

Fig.19. The function diagram of the digital double-edge PWM generator.

D. Power Stage

H-birdge power stage is used in the digital class D power amplifier system for obtaining a better power supply efficiency and system performance. The H-bridge power stage is shown in “Fig.20”.

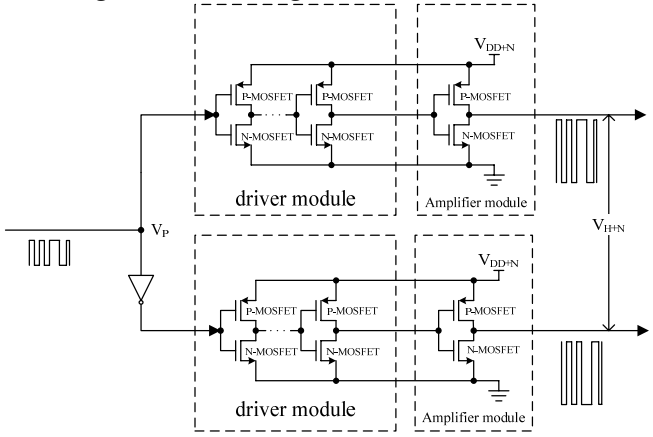

Fig20. H-bridge power stage.

V. SIMULATION RESULTS

When the input of the system is a -60dB 5000Hz sine wave and the power supply noise is a -40dB 500Hz sine wave, the system is simulated when the error correction block only corrects the error introduced by digital PWM block and corrects all error introduced by the system respectively. When the error correction block in the system only corrects the error introduced by digital PWM block, "Fig. 21" shows the output spectrum of the system, and SNR is 17.77dB. When the error correction block in the system corrects all error introduced by the digital PWM block and the power stage, "Fig. 22" shows the output spectrum of the system, and SNR is 45.17dB. When the input of the system is a -2dB 5000Hz sine wave, and under the condition that the amplitude of the power supply noise is -40 dB and the error correction block corrects all error, SNR of the system versus the frequency of the power supply noise is shown in "Fig. 23". When the input of the system is a -2dB 5000Hz sine wave, and under the condition that the frequency of the power supply noise is 500 Hz and the error correction block corrects all error, SNR of the system versus the amplitude of the power supply noise is shown in "Fig. 24".

The simulation results show that using the proposed error correction method can basically eliminate the error introduced by power supply noise whose frequency is less than 1000Hz and amplitude is less than -20 dB. Because the power supply noise's frequency and amplitude are usually much smaller than the input signal's, the proposed method is useful and practical.

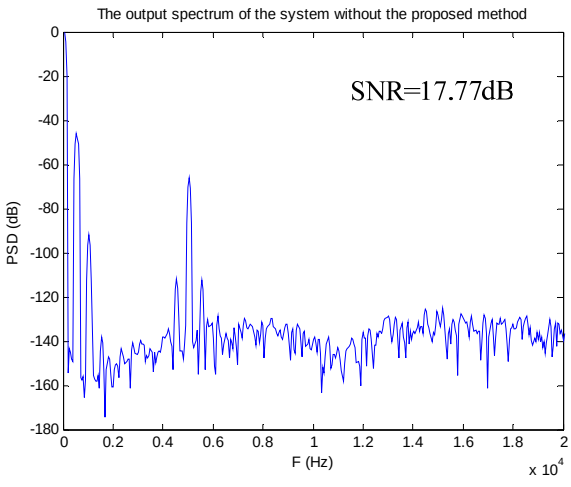

Fig. 21. The output spectrum of the system without the proposed method.

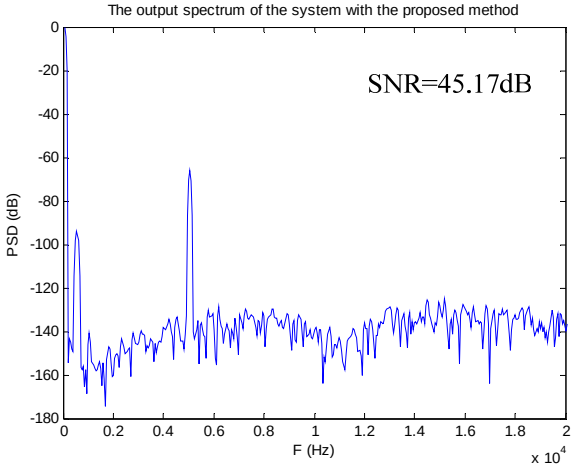

Fig. 22 The output spectrum of the system with the proposed method.

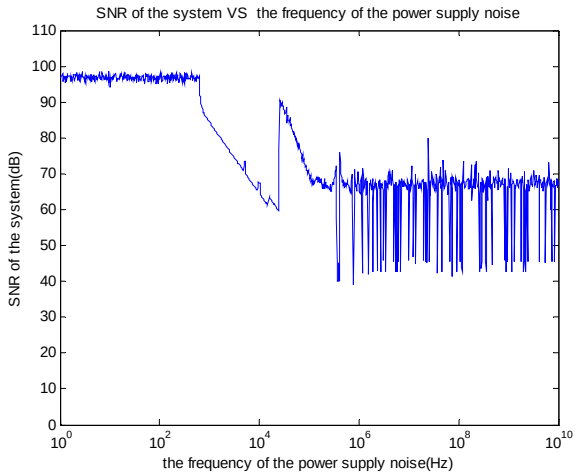

Fig. 23. SNR of the system versus the frequency of the power supply noise.

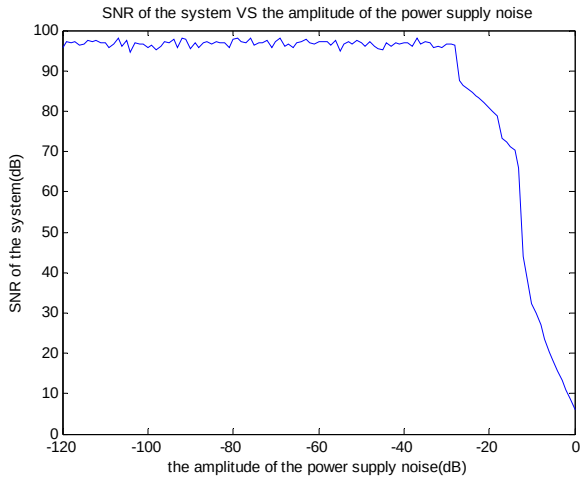

Fig. 24. SNR of the system versus the amplitude of the power supply noise.

VI. CONCLUSIONS

A method of error correction for power nosie in digital class D power amplifier is presented in this paper. A digital class D power amplifier with the proposed method can basically correct the error introduced in power supply noise, even when a single-ended power stage is used in the power amplifier to save the cost of the system. To verify the method, an audio digital class D power amplifier is designed and simulated in this paper. The simulation results in section Ⅳ indicate this method can eliminate the error produced by power stage and improve the performance of the system.

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